



Dual P-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

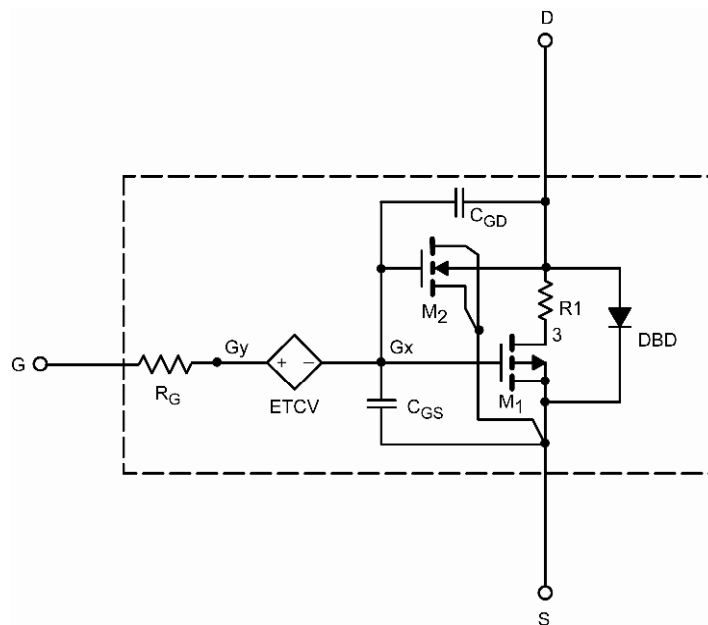
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model SiA911ADJ



Vishay Siliconix

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	0.83		V
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -2.8\ \text{A}$	0.097	0.096	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -2.3\ \text{A}$	0.126	0.126	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -2.8\ \text{A}$	7	7	S
Diode Forward Voltage	V_{SD}	$I_S = -1\ \text{A}$	-0.79	-0.80	V
Dynamic^b					
Input Capacitance	C_{iss}	$V_{DS} = -10\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$	332	345	pF
Output Capacitance	C_{oss}		75	65	
Reverse Transfer Capacitance	C_{rss}		61	50	
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -8\ \text{V}, I_D = -3.5\ \text{A}$	7	8.4	nC
		$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -3.5\ \text{A}$	4.2	4.9	
Gate-Source Charge	Q_{gs}		0.75	0.75	
Gate-Drain Charge	Q_{gd}		1.2	1.2	

Notes

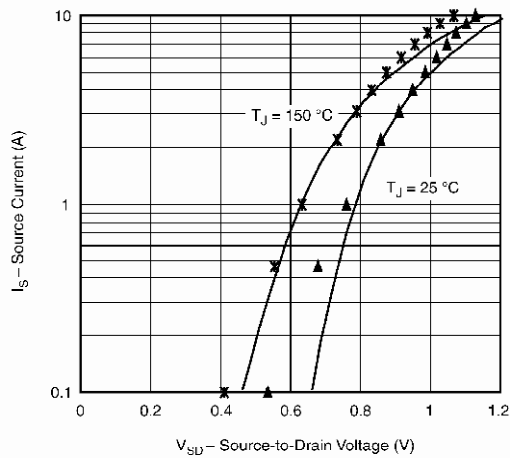
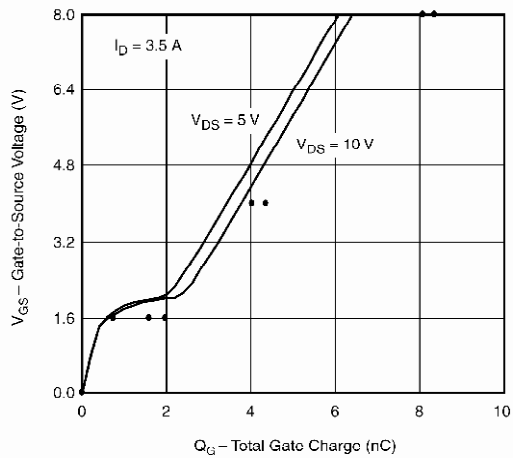
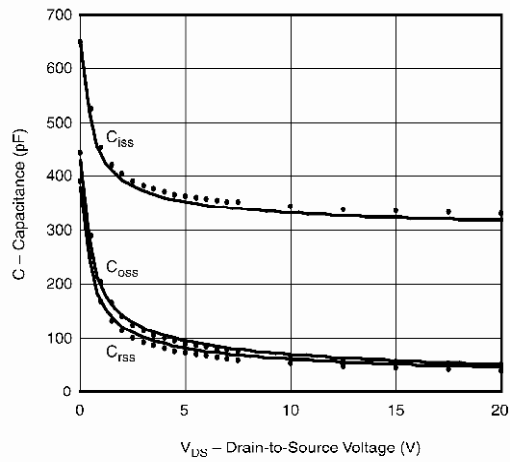
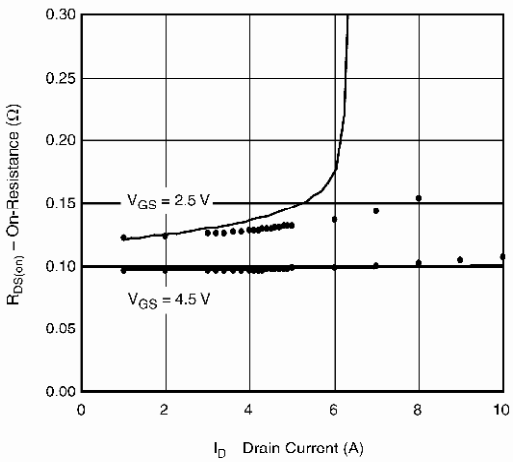
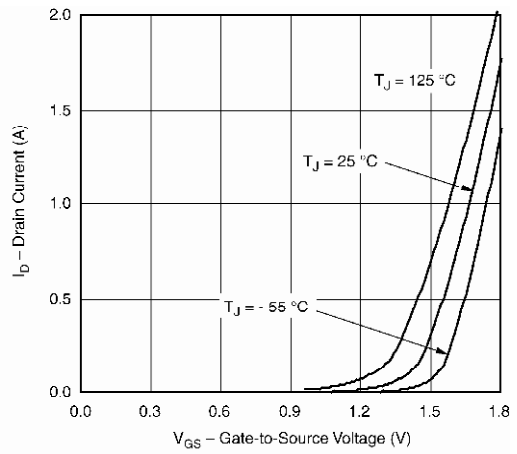
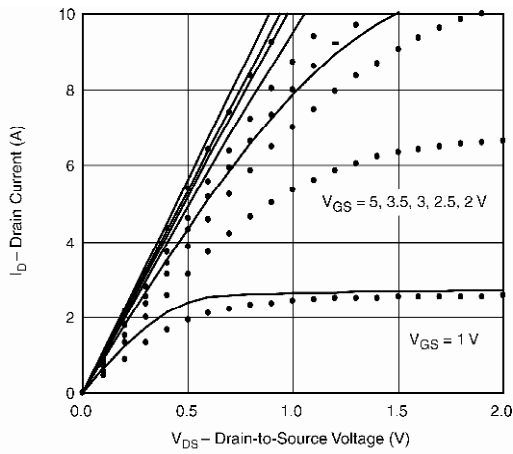
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.



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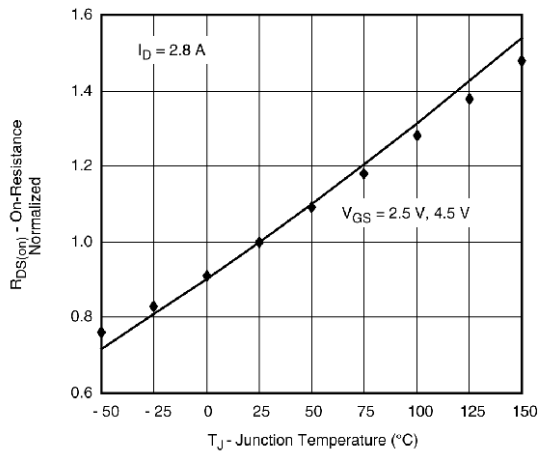
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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